Docket No. 030712-36

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 3838
Hiroki Goko	)	Examiner: MEMULA, Suresh
Application No. 10/813,031	)	Group Art Unit: 2825
Filed: March 31, 2004	)	
For: APPARATUS AND METHOD FOR DESIGNING SEMICONDUCTOR INTEGRATED CIRCUIT	)	Date: October 28, 2009

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the Pre-Appeal Brief Conference Pilot Program guidelines set forth in the July 12, 2005, Official Gazette Notice, Appellant hereby submits this Pre-Appeal Brief Request for Review of the final rejections of claims 1-5 in the above identified application.

Claims 1-5 were rejected in the Final Office Action dated April 28, 2009. Appellant filed a Request for Reconsideration on July 28, 2009, and the Patent Office issued an Advisory Action dated August 14, 2009 maintaining the final rejections of claims 1-5. Appellant hereby appeals these rejections and submit this Pre-Appeal Brief Request for Review.

Claims 1-5 were rejected under 35 U.S.C. §102(e) as being anticipated by Weaver, Jr. (US 2004/0230933 – hereinafter Weaver). The rejection is traversed as being clearly erroneous in that the cited reference fails to disclose all of features clearly recited in claims 1-5. In view of the clear error in the rejection, withdrawal thereof is respectfully requested.

According to the present invention, a method of designing semiconductor ICs comprises two separate routines, a circuit design routine and a layout design routine, as shown in Fig. 2 of the application. The circuit design routine is the first routine SUB1, and following the circuit design routine is a layout design routine SUB2.

Claim 1 is directed to the circuit design routine SUB1, which is shown in detail as substeps (e.g., SS16, SS20, SS22, and SS24) in Fig. 3, while dependent claim 2 is directed to the sequential layout design routine SUB2 shown in detail as substeps (e.g., SS34, SS36, SS38, SS40, and SS42) in Fig. 4.

The steps in SUB1 in Fig. 3 are performed before the steps in SUB2 in Fig. 4. Hence, the claimed steps 1st through 7th steps in claims 1 and 2 are performed in proper order as recited in the claims.

With Appellant's claimed method as recited in the steps of claims 1 and 2, for example, timing analysis is performed using the plural clocks even in the layout design (i.e., SUB2 steps) to make a decision as to whether violation of timing constraints has occurred, thereby making it possible to obtain a layout design that has satisfied all constraints, as discussed in lines 3-8 in page 20 of the specification.

In contrast with Appellant's claimed invention, Weaver generally describes an IC design methodology that applies manual pre-placement (i.e., layout) of certain critical circuit elements followed by circuit optimization based on timing estimates at an early stage in the design process. According to paragraph [0045] of Weaver, after the circuit design phase, the placed netlist (i.e., designed and optimized circuit) may be provided to a layout vendor, which then performs a full layout design of the completed design and optimized netlist. That is, Weaver is directed mainly to a design process with manual pre-placement of certain critical circuit elements at an early stage in the circuit design process, while leaving the main layout process to be performed by a layout vendor. Hence, Weaver does not follow the sequential or even

logical order nor include the combination of steps recited in claim 1 directed to a design process and claim 2 directed to a layout process, for example, in Appellant's claimed invention.

More specifically, as described in, e.g., paragraph [0014] of Weaver, the pre-placement process may involve locating and fixing strategic electrical infrastructure such as clock trees, ESD protection circuits, I/O circuit, etc., followed by automatic placement (i.e., layout) of the remainder of the chip circuits. The methodology of Weaver with pre-placement of critical electrical infrastructure (i.e., physical system layout) prior to a design phase is shown in the single drawing Fig. 1 of Weaver.

In maintaining the rejection, the Examiner contends that Appellant's claimed 2nd step for allocating clocks supplied to respective circuit is anticipated by Weaver's "element 6". That is, as contended by the Examiner, "element 6" of Weaver is interpreted as a circuit design step and not a layout design step. However, such an interpretation is contrary to the teachings of Weaver at least for the reasons explained below.

Appellant's claimed 2nd step in a method of designing semiconductor ICs that includes two separate routines. As shown in Fig. 2 of the application, the 2nd step is a part of a first routine SUB1, which is a circuit design routine. As mentioned previously, according to the claimed invention, following the completion of the circuit design routine (i.e., SUB1) is a layout design routine (i.e., SUB2).

In contrast with Appellant's 2nd step in the design routine, Weaver's "element 6" is related to the pre-placement (i.e., layout) of critical electrical infrastructure (i.e., physical system layout). According to Weaver, "element 6" performing a pre-placement or layout design step is an unconventional step in the midst of a circuit design phase, which begins in block 2 in Fig. 1 of Weaver.

Further, in Weaver there is "element 8" that provides a repeat of the pre-placement process 6 based on the condition of whether congestion is acceptable or not. This conditional repeat does not exist in Appellant's 2nd step. Therefore,

Appellant respectfully submits that there is no claimed step in the present invention that remotely suggests or is equivalent to the manual pre-placement of critical electrical infrastructure in "element 6" of Weaver.

Moreover, Appellant respectfully notes, e.g., paragraph [0034] of Weaver describing the pre-placement (i.e., layout) step in a circuit synthesis/design that begins in block 2 and continues in, e.g., block 10 and thereafter.

Further, according to Weaver's paragraph [0014], employing a layout design step (i.e., pre-placement of critical circuits) in an early stage of a circuit design phase is advantageous because the predictability of results is improved. That is, by performing a layout step (i.e., block 6) during the circuit design phase, problems with the critical components placement can be detected and solved early in circuit design. Thus, when a completed circuit design is provided to a layout vendor for a full layout, less problems and less redesign of circuit can be expected. As clearly recited in Appellant's claim 1 directed to a design process, there is no pre-placement or layout steps as required by Weaver's teachings.

As another example of misinterpretation of Weaver, the Examiner contends that "element 18", which is performed after the design process shown in elements 4, 6, 10, 14, and 16, corresponds to Appellant's layout sign process. However, Weaver specifically labels "element 18" as "route and parasitic extraction", which precedes "static timing analysis" block 20 in Weaver. Appellant respectfully asserts that there is no relationship between the "static timing analysis" block 20 of Weaver to Appellant's 4th step for generating clocks different in delay amount for the verification of a layout design.

Further, although Weaver shows a decision block 22 determining whether or not timing is met, there is no disclosure of adjusting skews and adjusting delays, as recited in Appellant's 5th and 6th steps, respectively.

Still further, the Examiner contends that "elements 10 and 22" of Weaver are equivalent to Appellant's 3rd step as well as the 5th and 6th steps. However,

Appellant's 3rd step is not interchangeable or equivalent to the 5th and 6th step. Hence, such a contention by the Examiner is illogical and insupportable.

Appellant respectfully acknowledges that Examiners are entitled to interpreting a reference broadly. However, the reference's teaching may not be taken out of context such that its original functionality is misapplied, such as in the case of the improper application/interpretation of Weaver.

In view of the arguments set forth above, each and every feature of the present claims is not taught (and is not inherent) in Weaver, as is required by MPEP Chapter 2131 in order to establish anticipation. Hence, the rejection of claims 1-5, under 35 U.S.C. §102(e), as anticipated by Weaver is improper.

Reconsideration and withdrawal of the rejection of claim 1-5, in view of clear errors in the Final Office Action, is respectfully requested.

Respectfully submitted,

STUDEBAKER & BRACKETT PC

/Donald R. Studebaker/
Donald R. Studebaker
Reg. No. 32,815

Studebaker & Brackett PC
One Fountain Square
11911 Freedom Drive
Suite 705
Reston, Virginia 20190
(703) 390-9051
Fax: (703) 390-1277
don.studebaker@sbpatentlaw.com